**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

1. (Original) A method for manufacturing a mask for integrated circuit devices, the method comprising:

providing a mask including a surface region, the surface region including a plurality of spaced regions forming an array configuration, each of the spaced regions being separated from each other by an opaque region to form the array configuration and being characterized by a dimension no greater than 0.25 microns;

selectively coding one or more of the spaced regions to define a masked read only memory (ROM) structure, each of the coded spaced regions including a structure, the structure causing an interference with light from a light source;

illuminating the surface region of the mask with the light source to allow the light to traverse through each of the spaced regions, whereupon the selectively coded one or more spaced regions transmits a lower light intensity to a photoresist material than a light intensity on the photoresist material from light illuminated on the photoresist material through the spaced regions free from the one or more codings; and

developing the photoresist material to selectively remove portions of the photoresist material only in the portions where light transmitted through the spaced regions free from coding while the portions of the photoresist material corresponding to the one or more coded regions remain intact.

2. (Original) The method of claim 1 wherein the structure is selected from a shifter or an anti-scattering bar.

3. (Original) The method of claim 1 wherein the one or more coded regions is characterized by a lower transmission rate than a transmission rate of the spaced regions free from coding.

4. (Original) The method of claim 1 wherein the integrated circuit device is a masked ROM.

5. (Original) The method of claim 1 wherein the photoresist material is overlying a semiconductor substrate.

6. (Original) The method of claim 1 further comprising processing exposed regions of the photoresist material.

7. (Original) The method of claim 1 wherein the light source is KrF source.

8. (Original) The method of claim 1 wherein the illuminating is a single exposure to form the ROM structure.

9. (Original) The method of claim 1 wherein the opaque region is MoSi or chromium.

10. (Original) The method of claim 1 wherein each of the spaced regions is characterized by a length of 0.2 microns.

11. (Original) A method for manufacturing a coded mask structure, the method comprising:

providing a mask substrate including a surface region, the surface region including a plurality of spaced regions forming an array configuration, each of the spaced regions being separated from each other by an opaque region, each of the spaced regions being separated by each other by a common dimension of no greater than 0.25 microns; and

selectively coding at least one of the spaced regions to define a mask for a read only memory (ROM) structure, the one coded spaced region being capable of causing an interference with a light source to transmit a lower intensity of light relative to any one of the spaced regions free from the coding.

12. (Original) The method of claim 11 wherein the coded spaced region including a structure, the structure being selected from a shifter or an anti-scatter bar.

13. (Original) The method of claim 11 further comprising using the mask for manufacturing a read only memory device.

14. (Original) The method of claim 11 further comprising illuminating a light from a KrF source through each of the spaced regions to form a pattern on a photosensitive material.

15. (Original) The method of claim 14 wherein the photosensitive material comprises a threshold.

16. (Original) The method of claim 11 wherein the mask substrate comprises a quartz material.

17. (Original) The method of claim 11 wherein each of the spaced regions includes a characteristic dimension of less than 0.2 microns.

18. (Original) The method of claim 11 wherein the opaque region comprises a chrome material.

19. (Original) A reticle structure for integrated circuit device, the reticle comprising:

a transparent substrate having a surface region;

a plurality of spaced regions on the surface region, each of the spaced regions being configured to form an array, the array having a plurality of rows that intersect a plurality of columns, each of the spaced regions being defined within a pair of rows and a pair of columns; whereupon each of the spaced regions being separated by each other by a common dimension of no greater than 0.25 microns; and

at least one of the spaced regions including a code to define a masked read only memory (ROM) structure, the one coded spaced region causes an interference with a light source to transmit a lower intensity of light relative to any one of the spaced regions free from the coding.

20. (Currently Amended) The ~~mask~~ reticle structure of claim 19 wherein the lower intensity of light prevents development of a photosensitive material.